REMARKS

Claims 1, 2, 7, 8, 15 and 17-31 are now pending in the application, with claims 1, 7 and 25 being the independent claims. Reconsideration and further examination are respectfully requested.

Initially, Applicants thank the Examiner for the indication that claims 20 and 21 would be allowable if rewritten into independent form so as to include all of the limitations of the base claim and any intervening claims. However, for the reasons set forth below, Applicants continue to believe that the other pending claims also should be indicated as being allowable and, therefore, have declined to amend claims 20 and 21 into independent form.

In the Office Action, Claim 1 has been rejected on the ground of nonstatutory obviousness-type double patenting over claim 1 of U.S. Patent No. 7,093,147 (the '147 patent) in view of U.S. Patent Publication No. 2003/0110012 (Orenstien); claim 7 has been rejected on the ground of nonstatutory obviousness-type double patenting over claim 14 of the '147 patent in view of Orenstien; claims 1, 2, 5, 6, 17-19 and 22 have been rejected under 35 U.S.C. § 102(e) over Orenstien; claims 7, 8, 11, 12 and 15 have been rejected under 35 U.S.C. § 103(a) over Orenstien in view of U.S. Patent No. 5,838,976 (Summers); claim 23 has been rejected under § 103(a) over Orenstien in view of an article titled, "Trends in Network and Pervasive Computing - ARCS 2002", April 2002 (Schmeck); claims 20and 21 have been rejected under § 103(a) over Orenstien in view of U.S. Patent 5,913,068 (Matoba); and claim 24 has been rejected under § 103(a) over Orenstien in view of U.S. Patent 6,986,141 (Diepstraten). Withdrawal of these rejections is respectfully requested for the following reasons.

At the outset, it is noted that many of the arguments made in the present Office Action previously were raised in the final rejection of January 17, 2008. Those arguments subsequently

were addressed in Applicants' Appeal Brief filed on June 4, 2008. For the sake of brevity, the points made by Applicants in the Appeal Brief are not repeated here. Rather, the following discussion only addresses the additional arguments that have been newly raised in the current Office Action.

Independent claim 1 is directed to a computer system comprising a plurality of computer processor cores in which at least two differ in processing performance, and in which all execute the same instruction set. The computer system also comprises a performance measurement and transfer mechanism that moves a plurality of executing computer processing jobs amongst the computer processor cores based on a measured throughput metric.

The foregoing combination of features is not disclosed or suggested by the asserted double-patenting combination. For instance, no permissible combination of claim 1 of the '147 patent and Orenstien would have disclosed or suggested at least the feature of moving a plurality of executing computer processing jobs amongst a plurality of computer processor cores based on a measured throughput metric.

This feature of the invention has been clarified in the claim amendments above[1]. Therefore, it is not addressed in its present form in the current Office Action.

Applicants have studied Orenstien in detail and are not able to find any teaching of any measured throughput metric. Rather, Orenstien merely discusses techniques for modifying certain parameters pertaining to process execution based on power-consumption and thermal considerations.

[1] Support for the amendment can be found, e.g., at page 5 lines 20-29 and in the Abstract (specifically, page 22 lines 11-17) of the Specification.

The Office Action refers to paragraph [0034] lines 1-2 of Orenstien which states, "...the sum module 275 ensures that processing throughput is increased to the extent possible given the desired thermal envelope." However, this statement must be read in conjunction with the rest of Orenstien's paragraph [0034] which, e.g., also states, "Voltages or frequencies to one or both of the cores may be ratcheted up in order to improve performance when the sum module detects that overall power consumption is below a selected power consumption metric."

In other words, in the portion of Orenstien referenced in the Office Action, Orenstien is describing a technique in which voltage or frequency is adjusted, subject to the desired thermal envelope. Such voltage and frequency adjustments naturally have some effect on processor speed and, accordingly, throughput as well. However, simply affecting throughput based on such voltage or frequency adjustments is significantly different than moving jobs amongst a plurality of computer processor cores based on a measured throughput metric, i.e., a measurement-based metric that reflects actual throughput itself.

Again, it appears that all of the processing in Orenstien is based on power-consumption and thermal considerations. Orenstien says nothing at all about any measured throughput metric, much less about moving a plurality of executing computer processing jobs amongst a plurality of computer processor cores based on such a measured throughput metric. Because its processing is based solely on power-consumption and thermal considerations, Orenstien would not have added anything to claim 1 of the '147 patent in relation to the present feature of the invention.

Accordingly, withdrawal of the double-patenting rejection is respectfully requested.

The same points apply to the present anticipation rejection of independent claim 1. That is, for the same reasons set forth above (and, as to arguments set forth in the previous Office Action, for the reasons set forth in the Appeal Brief), Orenstien does not disclose at least the

feature of moving a plurality of executing computer processing jobs amongst a plurality of computer processor cores based on a measured throughput metric.

The present Office Action asserts that the previously claimed feature was merely "an intended use limitation". While Applicants disagree with that characterization, the above amendments to the subject claim feature emphasize even more clearly that the feature is not an intended use limitation, but rather a structural limitation on the way different elements interact with each other. With respect to this feature, as pointed out above, Orenstien says nothing at all about any measured throughput metric, but instead only pays attention to power-consumption and thermal considerations.

Accordingly, withdrawal of the § 102 rejection of independent claim 1 is respectfully requested.

Independent claim 7 is directed to a method for operating multiple processor cores, comprising placing a plurality of computer processor cores on a single semiconductor die, in which at least two computer processor cores differ in processing performance, and in which all execute the same instruction set. A throughput metric that identifies throughput achieved by the computer processor cores as a function of workloads running on the computer processor cores is obtained, and individual ones of the computer processing jobs are transferred amongst targeted ones of the plurality of computer processor cores based on the throughput metric.

The foregoing combination of features is not disclosed or suggested by the asserted double-patenting combination. For instance, no permissible combination of claim 14 of the '147 patent and Orenstien would have disclosed or suggested at least the feature of transferring individual ones of a plurality of computer processing jobs amongst targeted ones of a plurality of computer processor cores based on a throughput metric that identifies throughput achieved by

the computer processor cores as a function of workloads running on the computer processor cores.

Once again, this feature of the invention has been clarified in the claim amendments above[2]. Therefore, it could not have been addressed in its present form in the current Office Action.

However, Applicants have studied Orenstien in detail and are not able to find any teaching of any throughput metric as presently recited. Rather, as noted above, Orenstien merely discusses techniques for modifying certain parameters pertaining to process execution based on power-consumption and thermal considerations. Therefore, Orenstien would not have added anything to claim 14 of the '147 patent in relation to the present feature of the invention.

Accordingly, withdrawal of the double-patenting rejection of independent claim 7 is respectfully requested.

In addition, no permissible combination of Orenstien and Summers would have disclosed or suggested at least independent claim 7's feature of transferring individual ones of a plurality of computer processing jobs amongst targeted ones of a plurality of computer processor cores based on a throughput metric that identifies throughput achieved by the computer processor cores as a function of workloads running on the computer processor cores.

As noted above, Orenstien does not say anything at all about the presently recited throughput metric. The Office Action refers to Orenstien's statement (in paragraph [0017]) that "hot" and "cool" processes can be swapped between hardware units. However, that paragraph of

[2] Support for the amendment can be found, e.g., at page 5 lines 20-29 and in the Abstract (specifically, page 22 lines 11-17) of the Specification.

Orenstien seems to indicate that such swapping is solely for the purpose of thermal management. It appears to be completely unrelated to the presently recited throughput metric.

The Office Action also asserts that "the result of the migration of jobs between the cores is an increase in throughput," citing page 4 paragraph [0033] lines 1-2 of Orenstien. However, that portion of Orenstien merely talks about monitoring overall power consumption, and the rest of paragraph [0033] notes that the monitored power can be used to control voltage and/or frequency supplied to the cores for the purpose of keeping within a desired power envelope. Although throughput certainly can be affected in this manner, doing so is significantly different than transferring computer processing jobs amongst computer processor cores based on a throughput metric according to claim 7. Once again, Orenstien does not even remotely suggest any throughput metric as presently recited, much less transferring computer processing jobs based on one.

The Office Action further asserts that it would have been obvious to modify Orenstien's system based on the teachings of Summers in order to achieve the above-referenced feature of the invention. However, while Summers does talk about measuring performance metrics, it does so for the purpose of allowing a software programmer to optimize software code at the design stage. See, e.g., column 1 lines 20-35 of Summers. Summers appears to be particularly interested in profiling code with respect to memory usage so that the programmer can avoid synchronization errors in which individual threads must waste time waiting for a particular memory cell to become available. See, e.g., column 4 lines 25-60 of Summers.

Because Summers is directed to a completely different problem (thread profiling for the purpose of developing optimized software code) than Orenstien (real-time thermal management), it is not believed that one of ordinary skill in the art would have had any motivation whatsoever

to combine the teachings of these two references. In addition, even if one attempted to combine their teachings, no permissible combination would have resulted in the presently recited features.

Accordingly, withdrawal of the § 103 rejection of independent claim 7 is respectfully requested.

The other rejected claims in this application depend from the independent claims discussed above, and are therefore believed to be allowable for at least the same reasons. Because each dependent claim also defines an additional aspect of the invention, however, the individual reconsideration of each on its own merits is respectfully requested.

New independent claim 25 is directed to a method for operating multiple processor cores. A throughput metric that identifies throughput achieved by computer processor cores on a single semiconductor die as a function of workloads running on such computer processor cores is obtained, and a plurality of computer processing jobs are assigned amongst the plurality of computer processor cores based on the throughput metric. At least two of the computer processor cores differ in size or complexity (e.g., as described at page 1 lines 12-14 of the Specification), but execute the same instruction set.

Thus, claim 25 is similar to independent claim 1, discussed above, and is believed to be allowable for similar reasons. New dependent claims 26-31 also are similar to claim 1's dependent claims and are believed to be allowable for similar reasons to those set forth in Applicants' previous Appeal Brief.

In order to sufficiently distinguish Applicants' invention from the applied art, the foregoing remarks emphasize several of the differences between the applied art and Applicants' invention. However, no attempt has been made to categorize each novel and unobvious difference. Applicants' invention comprises all of the elements and all of the interrelationships

between those elements recited in the claims. It is believed that for each claim the combination of such elements and interrelationships is not disclosed, taught or suggested by the applied art. It is therefore believed that all claims in the application are fully in condition for allowance, and an indication to that effect is respectfully requested.

If there are any fees due in connection with the filing of the currently submitted papers that have not been accounted for in this paper or the accompanying papers, please charge the fees to Deposit Account No. 08-2025. If an extension of time under 37 C.F.R. 1.136 is required for the filing of any of the currently submitted papers and is not accounted for in this paper or the accompanying papers, such an extension is requested and the fee (or any underpayment thereof) should also be charged to the Deposit Account.

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Respectfully submitted,
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